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EXAMINER

GANDHI, DIPAKKUMAR B

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/853,260

Applicant(s)

LOEWEN, MYRON09853260

Examiner

Dipakkumar Gandhi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7 and 10-14 is/are allowed.
- 6) ☒ Claim(s) 1-6 and 15-26 is/are rejected.
- 7) ☒ Claim(s) 8 and 9 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner *for the abstract contains legal phraseology.*
- 10) ☒ The drawing(s) filed on 11 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6/19/01.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

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DETAILED ACTION

Claim Objections

1. Claims 8 and 9 are objected to because of the following informalities: Claims 8 and 9 should be dependent on claim 7, as the functional units (in claim 8 and 9) are mentioned in claim 7 and not in claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-6, 15-18, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (US 4,528,665) in view of Beatty et al. (US 4,562,550), Allinger et al. (US 2002/0191733 A1) and Hayashi et al. (JP 07093505 A).

As per claim 1, Burns et al. teach a counter arrangement (figure 9a, 9b, col. 3, lines 40-41, col. 10, lines 5-7, Burns et al.) wherein the counter control means (figure 1B, col. 5, lines 20-24, Burns et al.) change the content of only one of the counter registers for each change in the counting sequence (col. 7, lines 18-20, Burns et al.).

However Burns et al. do not explicitly teach the specific use of means to update the checksum registers and a function performed on the content of all checksum registers results in a constant value.

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Beatty et al. in an analogous art teach that the number of bytes received is calculated by taking the 1's complement of the sum of the down-counting byte counter register plus the 1's complement of 7. The checksum register is initialized to a value of 80H. A byte from the receiver buffer is then summed into the checksum register. When all bytes have been checked, then a test is made to determine if the final checksum value is equal to 0 (col. 28, lines 39-42, lines 44-47, lines 54-56, Beatty et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns et al.'s patent with the teachings of Beatty et al. by including an additional step of using a plurality of counter registers and at least the same number of checksum registers and comprise means to update the checksum registers and a function performed on the content of all checksum registers results in a constant value.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect an error in the counter registers and recover the value of the counter registers.

Burns et al. also do not explicitly teach specifically that the content of each checksum registers is defined by an associated function, which allows recovery of the content of each counter register.

However Allinger et al. in an analogous art teach that the counting value of the single-stage auxiliary counter is recovered in the checking device resulting in a recovered counting value (page 1, paragraph 8, Allinger et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns et al.'s patent with the teachings of Allinger et al. by including additionally that the content of each checksum registers is defined by an associated function, which allows recovery of the content of each counter register.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide redundancy and to recover the content of a counter.

Burns et al. also do not explicitly teach the specific use of a plurality of counter registers and at least the same number of checksum registers.

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However Hayashi et al. in an analogous art teach that the total counter data of the register A3 and the checksum of the register B4 are checked in the comparing and judging part 7, the total counter data of the register C5 and the checksum of the register D6 are checked in the comparing and judging part 8 (abstract, Hayashi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns et al.'s patent with the teachings of Hayashi et al. by including an additional step of using a plurality of counter registers and at least the same number of checksum registers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the contents of the counter registers.

- As per claim 2, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Hayashi et al. teach the counter arrangement, wherein respective sets of two counter registers from the plurality of counter registers are coupled with an associated checksum register through a functional unit (abstract, Hayashi et al.).

- As per claim 3, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Hayashi et al. teach the counter arrangement, wherein the functional unit performs a logical function (abstract, Hayashi et al.).

- As per claim 4, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Hayashi et al. teach counter arrangement, wherein the functional unit performs an arithmetic function (Detailed description, paragraph 3, Hayashi et al.).

- As per claim 5, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Burns et al. teach the counter arrangement, wherein the functional unit is an EXCLUSIVE OR gate (col. 13, lines 44-49, Burns et al.).

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- As per claim 6, Burns et al., Beatty et al. and Allinger et al. teach the additional limitations. Burns et al. teach counter arrangement, wherein the control unit comprises an incrementer/decrementer unit selectively coupled with one of the counter registers (col. 7, lines 18-20, Burns et al.).
- As per claim 15, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Burns et al. teach a method for operating a counter (figure 9a, 9b, col. 3, lines 40-41, col. 10, lines 5-7, Burns et al.) and changing the value of only one of the counter registers with every change in a counting sequence (col. 7, lines 18-20, Burns et al.).

Hayashi et al. teach a plurality of counter registers and at least the same number of checksum registers and calculating the value of the associated checksum registers as a function of the content of at least two counter registers (abstract, Hayashi et al.).

Beatty et al. teach that a checksum calculated from all checksum registers results in a constant value (col. 28, lines 39-42, lines 44-47, lines 54-56, Beatty et al.).

- As per claim 16, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Hayashi et al. teach a method, wherein a logical function is used (abstract, Hayashi et al.).

- As per claim 17, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Hayashi et al. teach a method wherein an arithmetic function is used (Detailed description, paragraph 3, Hayashi et al.).

- As per claim 18, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Burns et al. teach a method, wherein an EXCLUSIVE OR function is used (col. 13, lines 44-49, Burns et al.).

- As per claim 22, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

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Burns et al. teach a method, wherein changing the value of one counter registers comprises the step of incrementing the value of the register by "1" (col. 7, lines 18-20, lines 23-26, Burns et al.).

- As per claim 23, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Burns et al. teach a method, wherein changing the value of one counter registers comprises the step of decrementing the value of the register by "1" (col. 7, lines 18-20, lines 23-26, Burns et al.).

- As per claim 24, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. teach the additional limitations.

Burns et al. teach a method, wherein changing the value of one counter registers comprises the step of using a gray code for increments or decrements (col. 7, lines 18-20, lines 23-26, Burns et al.).

5. Claim 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (US 4,528,665), Beatty et al. (US 4,562,550), Allinger et al. (US 2002/0191733 A1) and Hayashi et al. (JP 07093505 A) as applied to claim 15 above, and further in view of Meckstroth et al. (US 4,091,449).

As per claim 19, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. substantially teach the claimed invention described in claim 15 (as rejected above). Burns et al. also teach incrementing or decrementing the binary code (col. 7, lines 23-26, Burns et al.).

However Burns et al., Beatty et al., Allinger et al. and Hayashi et al. do not explicitly teach the specific use of converting the content of all counter registers into binary code and converting said changed binary code back.

Meckstroth et al. in an analogous art teach the converting of Gray code weight readings to binary coded decimal form as indicated by the block 1208 and performed by the CDCH routine on page 10 of Table V. Table VI shows the conversion relationship between the special Gray code used and Binary coded decimal code (col. 28, lines 45-48, col. 57, lines 10-13, Meckstroth et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns et al.'s patent with the teachings of Meckstroth et al. by including an additional step of converting the content of all counter registers into binary code and converting said changed binary code back.

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This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to increment or decrement the value in the counter register in the binary format.

- As per claim 20, Burns et al., Beatty et al., Allinger et al., Hayashi et al. and Meckstroth et al. teach the additional limitations.

Meckstroth et al. teach a method, wherein the step of converting the content into binary code comprises the steps of: (a) selecting a most significant register (col. 19, lines 49-50, Meckstroth et al.); (b) testing whether the content of the selected register is odd (col. 52, lines 56-58, Meckstroth et al.); and if yes, inverting the content of the following register (col. 58, lines 34-38, Meckstroth et al.); (c) ending the conversion if the following register is the least significant register; (d) otherwise selecting the following register and repeating steps (b) through (d) (col. 38, lines 64-68, Meckstroth et al.).

- As per claim 21, Burns et al., Beatty et al., Allinger et al., Hayashi et al. and Meckstroth et al. teach the additional limitations.

Meckstroth et al. teach a method, wherein the step of converting the content from binary code comprises the steps of: (a) selecting the register preceding the least significant register (col. 19, lines 53-54, Meckstroth et al.); (b) testing whether the content of the selected register is odd (col. 52, lines 56-58, Meckstroth et al.); and if yes, inverting the content of the following register (col. 58, lines 34-38, Meckstroth et al.); (c) selecting the preceding register and repeating steps (b) through (c), (col. 27, lines 9-10, Meckstroth et al.).

6. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (US 4,528,665), Beatty et al. (US 4,562,550), Allinger et al. (US 2002/0191733 A1) and Hayashi et al. (JP 07093505 A) as applied to claim 15 above, and further in view of Young et al. (US 5,493,581).

As per claim 25, Burns et al., Beatty et al., Allinger et al. and Hayashi et al. substantially teach the claimed invention described in claim 15 (as rejected above).

However Burns et al., Beatty et al., Allinger et al. and Hayashi et al. do not explicitly teach the specific use of a method, wherein changing the value of the counter registers comprises the step of: (a) incrementing a first register to its maximum value for each value change; (b) incrementing a second register for the

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next value change; (c) decrementing the first register to its minimum value for each following value change; (d) incrementing the second register for the next value change; (e) repeating steps (a) through (d).

Young et al. in an analogous art teach that FIG. 11 schematically shows in block format phase generator 308 which includes phase accumulator 1102 with its 18 most significant bits fed to sin/cos generator 306, phase increment accumulator 1106 with output the phase increment on each Clock cycle, control 1108, comparator 1110 for chirp excursion endpoint detection, adder/subtractor 1112 for chirp increment/decrement, adder/subtractor 1114 for incrementing/decrementing the phase accumulator 1102 value with the phase increment value from phase increment accumulator 1106, register 1130 for holding the delta phase increment for chirp use, register 1132 for holding the minimum phase increment, register 1134 for holding the maximum phase increment on chirp excursions, and register 1104 for holding the phase offset to initialize phase accumulator 1102 (figure 11, col. 10, lines 22-36, Young et al.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Burns et al.'s patent with the teachings of Young et al. by including an additional step of using a method, wherein changing the value of the counter registers comprises the step of: (a) incrementing a first register to its maximum value for each value change; (b) incrementing a second register for the next value change; (c) decrementing the first register to its minimum value for each following value change; (d) incrementing the second register for the next value change; (e) repeating steps (a) through (d).

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to increment or decrement the value in the counter register to maximum or minimum value.

- As per claim 26, Burns et al., Beatty et al., Allinger et al., Hayashi et al. and Young et al. teach the additional limitations.

Young et al. teach a method, wherein changing the value of the counter registers comprises the step of: (a) decrementing a first register to its maximum value for each value change; (b) decrementing a second register for the next value change; (c) incrementing the first register to its minimum value for each

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following value change; (d) decrementing the second register for the next value change; (e) repeating steps (a) through (d), (figure 11, col. 10, lines 22-36, Young et al.)

Allowable Subject Matter

7. Claims 8-9 would be allowable if rewritten or amended to overcome the objection set forth above, see supra paragraph 1.

8. Claims 7-14 are allowable over the prior art of record.

9. The following is an examiner's statement of reasons for the indication of allowable subject matter:

The present invention relates to a method and apparatus for a counter arrangement with recover function realized within a microcontroller or microprocessor or a stand-alone counter arrangement usable in many applications, such as a digital odometer.

The claimed invention (claim 7) recites features such as: Counter arrangement comprising: a control unit; first, second, and third registers coupled with said control unit; fourth, fifth, and sixth registers coupled with said control unit; first, second, and third functional units each having two inputs and an output; wherein the inputs of the first functional unit being coupled with the first and second register, respectively and the output with the fourth register; the inputs of the second functional unit being coupled with the second and third register, respectively and the output with the fifth register; the inputs of the third functional unit being coupled with the first and third register, respectively and the output with the sixth register; and wherein the control unit performs a counter function on the first, second, and third registers such that the content of only one of the counter registers changes for each change in a counting sequence.

The prior arts of record teach a memory refresh system that incorporates a Gray code counter circuit for use as the memory refresh counter, and further includes error detecting circuitry for detecting erroneous operation of the refresh counter (Burns et al. US 4,528,665 is an example of such prior arts). The prior arts, however, do not teach coupling various registers, a control unit, inputs and outputs of the functional units as mentioned in claim 7. Hence the prior arts of record do not anticipate or render obvious the claimed invention. Thus, claim 7 is allowable over the prior arts of record. Claims 8-14 are dependent on claim 7. Hence, claims 8-14 are allowable over the prior arts of record.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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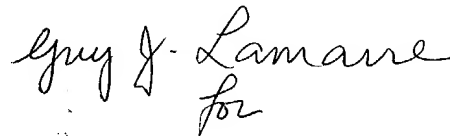
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Dipakkumar Gandhi
Patent Examiner



Albert DeCady
Primary Examiner